21.4 A Single-Power-Supply 0.7V 1GHz 45nm SRAM with An Asymmetrical Unit-β-ratio Memory Cell

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A single-power supply 64kB SRAM is fabricated in a 45nm bulk CMOS technology. The SRAM operates at 1GHz with a 0.7V supply using a fine-grained bitline segmentation architecture and with an asymmetrical unit-β-ratio 6T cell. With the asymmetrical cell, we save 22% cell area compared to a conventional symmetrical cell. This bulk SRAM is designed for GHz-class sub-1V operation (Fig. 21.4.1).

Low-voltage SRAM is one of the most important components of low-power mobile products, such as cell phones and mobile game machines, which often process large amounts of data. This creates demand for high-performance SRAM that supports low-voltage operation. However, ensuring the functionality and performance of SRAM is becoming more difficult because of the larger characteristic variability on cell transistors caused by technology scaling. Various circuit techniques have been proposed to conquer the influence of the variability. In some papers multiple-power-supply schemes are introduced [1-3]. However, these schemes make chip design more complicated and make chips more expensive. On the other hand, SOI technology is a good option for high-performance SRAM [4-7]. Nevertheless the history effect caused by PD-SOI often worsens the influence of the variability. As shown Fig. 21.4.1, 8T cells are used to build low-voltage SRAM with SOI [5,7], but the 8T cells require more area than 6T cells. Therefore, with a bulk process widely used as a standard technology, we fabricate a single-power-supply 6T SRAM that achieves 1GHz operation at 0.7V.

Figure 21.4.2 shows the DC simulation results of cell stability (CS) and write margin (WM) in a high-performance SRAM cell in 45nm technology. The assumed operating voltage range at SRAM cell is 0.9 to 1.1V. As shown in the figure, the degradation of WM due to the voltage scaling is more significant than that of the CS. The write failure rate is about 10^4 times larger at 0.7V than that at 0.9V. Cell current (I_{cell}) simulation results are also shown in this figure. I_{cell} decreased by 84% going from 0.9 to 0.7V for the worst case. This means that read-current degradation is also a severe issue for the low-voltage operation. Therefore, we first focus on improving WM and I_{cell}.

To improve WM, the drive ratio of the access transistor to the pull-up transistor needs to be increased. The enhancement of the access transistor drive-ability also increases I_{cell}. The access transistor is designed to have exactly the same size as the pull-down transistor, making this a unit β-ratio cell. In layout, this makes the edge line of the NMOS active area straight and the length of the all transistor channels identical. Consequently, we improve the robustness for the manufacturing [3]. As a result, both WM and I_{cell} improve by using the unit β-ratio cell. V_t of the cell transistors is lowered to improve both I_{cell} but WM. Even if we lower V_t, the increase of the leakage current is partially suppressed by the voltage scaling from 1.0V to 0.7V. This is because drain-induced barrier lowering (DIBL) is reduced by voltage scaling. Even though the increased current is not compensated by DIBL completely, we lower V_t by 60mV, avoiding the increase in leakage power dissipation. As shown in Fig. 21.4.2, we improve the minimum operating voltage by 130mV with these modifications. I_{cell} is also increased by 2.87× compare to the original cell. On the other hand, CS is ruined with these changes, and I_{cell} is still not high enough to achieve 1GHz operation. Therefore, we have to improve CS and I_{cell} without degrading WM.

To improve CS, we introduce a fine-grained bitline segmentation (FBLS) scheme. Measured and simulated CS failure dependencies on supply voltage are shown in Fig. 21.4.3. There is a good match between measured and simulated results. The DC measurements and simulations of CS give pessimistic results compared to the dynamic ones. Moreover CS improves when the cell count per bitline (BL) is decreased. This is because fast BL signal development rate due to the small BL capacitance helps memory cells to keep the stored data against disturbance. And the FBLS scheme does not degrade WM. We use transient simulation to estimate CS and WM hereafter because the DC simulation does represent CS correctly, particularly for the FBLS scheme [8]. We use single-ended read with this scheme to make use of the fast signal development owing to the small BL capacitance. With this read scheme, the access time is reduced by increasing the drive strength of the corresponding side of the BL pair and this makes the memory cell asymmetrical (Fig. 21.4.4). Generally, the asymmetry of the memory cell degrades CS and WM. But in this case, the effect of the variability reduction due to the transistor enlargement overwhelms the influence of symmetry distortion. The width of NMOS is increased 3.7× to achieve 1GHz operation. We save the 22% of the cell area, compared to the symmetrical cell with both NMOS enlarged. The cell area is $0.4997\mu m^2$ ($1.315\times0.380\mu m^2$) using asymmetry, but it is still as twice big as the 45nm low-cost version SRAM cell area. The reason is that the transistor width is enlarged to get enough I_{cell} for 1GHz operation at 0.7V and that we use relaxed design rules for non-immersion lithography to simplify the fabrication. With design rules for an immersion-lithography 45nm process, a cell area of $0.39\mu m^2$ is estimated for our cell. The cell count per BL is determined by optimizing the trade-off among area, speed and CS and 16 cells per BL is chosen for our case. The improvements due to the techniques mentioned above are summarized in Fig. 21.4.4.

Figure 21.4.5 shows the array configuration. The 64kB array consists of 128 identical 4kb sub-arrays. Each sub-array has local read and write circuits on opposite ends, and each circuit is shared with the adjacent sub-arrays. This placement relaxes the wire-congestion in the read/write circuit. It also makes local BLs shorter, improving CS and the BL signal development rate. Each local read/write circuit is connected to global read/write data line and the global read/write circuits are located in the middle of the array to reduce the delay of global data lines. The lower cell-area efficiency of FBLS is compensated by the smaller size of the local single-ended read circuit compared to the conventional sense amplifier. Also optical dummy cells are eliminated by OPC optimization. The SRAM macro area is $0.832mm^2$ ($1040\times800\mu m$) (Fig. 21.4.7), which is estimated to be 18% smaller than that of FBLS SRAM with conventional sense amplifier circuits. Fig. 21.4.6 shows simulated waveforms of the read and write operation.

Acknowledgment:
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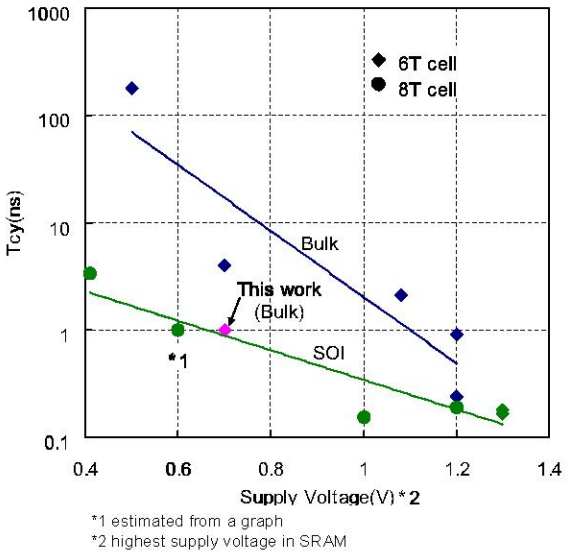


Figure 21.4.1: SRAM comparison of cycle time vs. supply voltage.

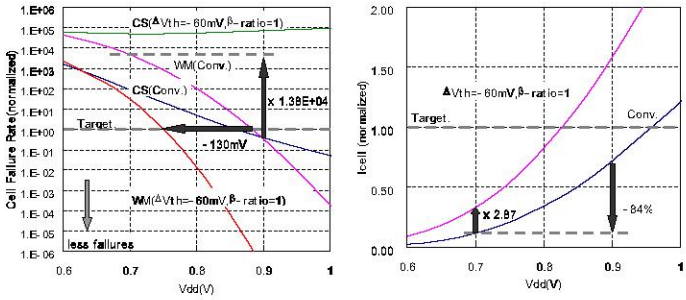


Figure 21.4.2: Simulated cell failure rate and I_{cell}.

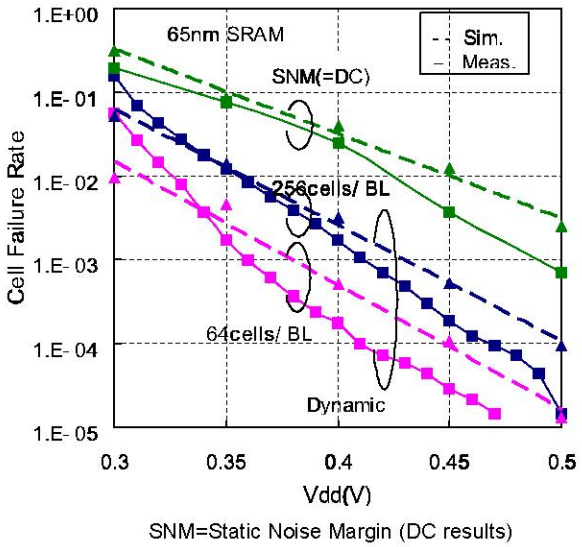
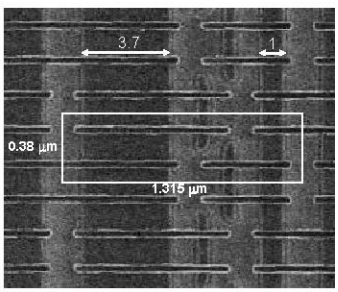


Figure 21.4.3: Measured and simulated cell stability (CS) failure rate.



Cell Failure Rate (Vdd=0.7V)

	Conv. (scaled)	This work (scaled)
CS	8.90 x 1E2	0.185
WM	4.57 x 1E4	1.00

Icell (Vdd=0.7V)

	Conv. (scaled)	This work (scaled)
Icell	0.11	1.00

Figure 21.4.4: Micrograph of the asymmetric cell and cell failure rate and I_{cell} comparison.

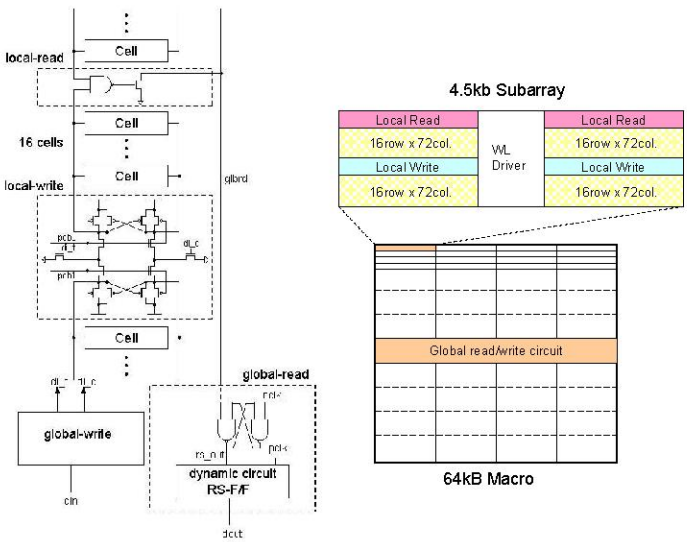


Figure 21.4.5: The array configuration and read/write circuits.

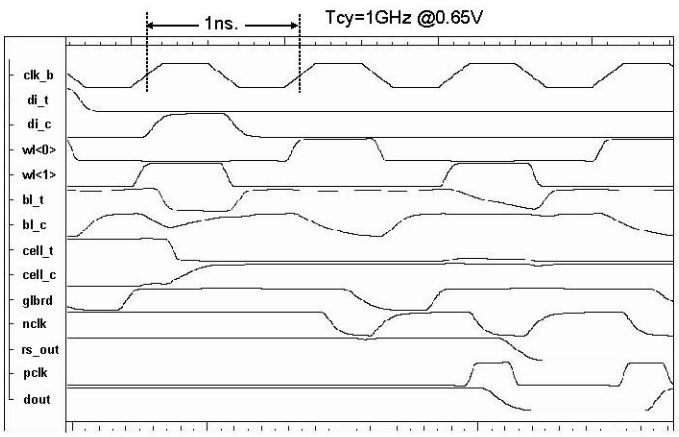


Figure 21.4.6: Simulated waveforms of write-read-read sequence.

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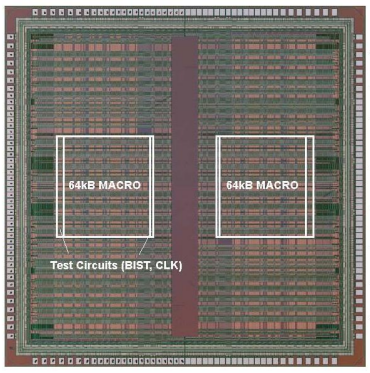

Organization	4kx140, 2kx280
Cycle time	1GHz
Power supply	0.7V
Technology	45nm CMOS w/ 8Metal
Design Rule	45nm non-immersion
Cell size	0.4997μm²
SRAM size	0.832mm²

Fig. 21.4.7: Chip micrograph and features.

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